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DIGITAL FM DEMODULATOR WITH REDUCED QUANTIZATION NOISE

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to digital frequency-modulation (FM) demodulation and more particularly, to a digital FM demodulator that extracts a digital time sequence from an intermediate frequency (IF) carrier while reducing quantization error and eliminating a requirement of a reference clock.

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2. Description of the Prior Art

Frequency modulation (FM) is an important and common method of information conveyance in radio communication systems. The receiver end of the system contains the FM demodulation circuit which is often of analog including a detector circuit and a phase lock loop (PLL) circuit. Often, the necessary circuitry to implement an FM demodulator is constructed on an integrated circuit chip. If the detector is brought into the integrated circuit, then a larger chip area is required. If the PLL is built into the integrated circuit, then an external capacitor is necessary outside the chip.

If the modulated signal requires digital signal processing after demodulation, then the circuit described above requires an analog-to-digital converter to convert

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the demodulated analog signal into digital signal. The analog signal is easily int ered with by noise. To reduce noise, the digital FM demodulator will first co rt the modulated intermediate-frequency (IF) signal into a digital signal by way of an analog-to-digital converter, thereafter using a digital signal processor to de ulate the modulation signal. The analog-to-digital converter and digital si processor used in the conventional digital FM demodulator must operate at hi speed to demodulate the modulation signal in real time. The system could use a ence clock with a multiple-fold frequency of modulation signal for sampling th ut signal to detect its phase change and then demodulate the signal, but such te ology requires a high frequency reference clock.

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he conventional methods of digital RF communication always need to co t the analog signal into digital signal in the receiver end with the drawbacks o reasing the circuit complexity. Thus, a demodulation circuit combining the de r circuit of a PLL with a carefully chosen analog-to-digital circuit to reduce qua tization error could result in accurate demodulation while simplifying circuit de n.

SUMMARY OF THE INVENTION

It is therefore a primary objective of the present invention to provide a new digital FM demodulator applicable to radio communication systems such as pagers, cellular phones, Global Positioning Satellite (GPS) systems, and Digital Enhanced Cordless Telecommunication (DECT) systems.

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The next objective of the present invention is to provide a digital FM demodulator implemented with an analog-to-digital converter. The input intermediate-frequency signal passes through the inventive demodulator thereby generating a digital signal including a high-frequency quantization noise signal. Then, by way of a low-pass filter, the quantized noise signal is filtered to acquire the baseband signal.

A further objective of the present invention is to provide a digital FM demodulator which adapts a PLL structure and utilizes the concept of delta-sigma analog-to-digital conversion which does not require external components or a high frequency reference clock.

The present invention provides advantages over similar systems in the prior art by using delay lines as the timing reference and by adapting the concept of delta-sigma analog-to-digital conversion to achieve the time-to-digital conversion of digital FM demodulation. This digital FM demodulator includes delay lines, an m-to-1 multiplexer, a phase detector, a charge pump circuit, a quantizer and a

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digital integrator. The modulation signal on an intermediate frequency carrier passes through the delay lines, each having a delay time of around one cycle time, and the phase of the delayed signal is compared with the phase of the original signal. This comparison produces a pulse which is applied to the charge pump circuit where a cumulative charge is stored in a capacitor. This charge is quantized into a voltage level which is accumulated by the digital integrator. Then, a new sample of another output signal of the delay lines is taken and compared in phase with the input signal. This system is similar to a PLL, i.e., it is a feedback system taking phase as the error signal. The quantized digital signal will feed through the low-pass filter defined by the sampling rate in the system to filter out high frequency noise and get the original modulation signal, i.e., the modulation signal is the digital output signal.

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BRIEF DESCRIPTION OF THE DRAWINGS

The drawings disclose an illustrative embodiment of the present invention, which serve to exemplify the various advantages and objects thereof, and are as follows:

Fig.1 is the circuit block diagram of the digital FM demodulator according to the present invention.

Fig.2 is the circuit waveform of the digital FM demodulator according to the present invention.

Fig.3 is the system structure of the digital FM demodulator according to the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

Please refer to Fig.1, which illustrates the circuit block diagram of the digital FM demodulator. The modulation signal, Ai(t), is fed into reference delay lines 11, said reference delay lines 11 including coarse delay line 111 and fine delay line 112. The delay times of delay lines 111 and 112 are controlled separately by other circuits. The fine delay lines 112 have multiple output signals Ai1(t), Ai2(t), Ai3(t)...Aij(t) which could be expressed as follows:

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$Aij(t)=Ai(t-Tc-j*\tau)$,

where,

Tc is the total fixed delay time of the coarse delay lines, and

τ is the unit delay time of fine delay lines.

The m-to-1 multiplexer 12 selects one of the output signals Ai0(t), Ai1(t), Ai2(t),..., Aij(t) from fine delay lines 112 as delayed signal, Aid. The phase detector 13 compares the phase difference between Aid and Ai, then generates an up or down signal. If the rising edge of Aid leads the Ai signal, the up signal will be generated as an effective pulse having a pulse width equivalent to the time difference between the rising edges of Ai and Aid, and the down signal will not be generated. The total delay time impressed on the Ai signal by passing through the delay lines is "Tc+d*τ", and the pulse width will equal to "T-Tc-d*τ" where d is the number of fine delay lines and "Tc+d*τ" is smaller than period T of the Ai

signal. Similarly, if the rising edge of Aid lags the Ai signal, a down signal pulse having a pulse width equal to the time difference of Aid and Ai, i.e., the pulse width will be equal to "Tc+d*τ-T".

The phase detector output value is considered positive when Aid leads the Ai signal, while its value is considered negative when Aid lags the Ai signal. The pulses of the up and down signals are applied to trigger the charge pump circuit 14 for charging and discharging a capacitor, Cc, which generates a voltage difference, Vf, the voltage level of which is proportional to the time difference or phase difference of the Aid and Ai signals. Each cycle of the modulated input signal will generate a Vf which is accumulated in storage capacitor Cc. The stored voltage will be quantized by quantizer 15 to generate a bit stream digital signal y(k), which is the output digital sequence of the total system.

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Quantizer 15 is a analog-to-digital converter which may be a one-bit or multiple-bit converter. A one-bit converter may be implemented by a voltage comparator. In the preferred embodiment, the quantizer 15 is a one-bit voltage comparator.

Digital integrator 16 accumulates the output digital signal y(k). In the preferred embodiment, digital integrator 16 is an up-down counter taking the output of quantizer 15 as its input. The counter output signal will select one output Aid signal from the fine delay lines by way of multiplexer 12. Thus, the delay time

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of the Aid signal is controlled by output signal y(k). The applied delay will be increased by one unit time if y(k)=1. Conversely, the delay of Aid will decrease one unit delay if y(k)=0. Thus, the system functions similarly to a PLL. The output signal y(k) is fed back to adjust the Aid delay time and make the next rising edge of Ai signal arrive at phase detector 13 simultaneously with the rising edge of Aid. The Aid signal is delayed by one cycle of the Ai signal when the system is locked.

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Referring to Fig.2, the circuit waveforms of the digital FM demodulator according to the present invention are shown. T(k) is the kth cycle time of the modulated input signal and P(k) is the time difference of rising edge of Aid and the next Ai cycle. The effective pulse of the up signal means P(k) is a positive value, and the down signal makes P(K) negative. Because the maximum frequency shift of input modulation signal is much smaller than carrier frequency, the change of T(k) is small relative to carrier cycle Tc. The effective pulse of the up signal and the down signal only happens at the rising edge of Aid and Ai signals and the effective pulse is transferred to Vf in storage capacitor Cc by way of charge pump circuit 14 before the arrival of the falling edge. The falling edge of Ai could be used as the trigger clock of the quantizer 15 and counter 16. Thus, the system does not require an external reference clock.

Using the waveform diagram of Fig.2, a formula may be developed as follows :

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$P(k+1)=P(k)+T(k)-T(k-1)+y(k)*\tau$,

where

$\Delta T(k)=T(k)-T(k-1)$.

Therefore, we could get

$P(k+1)=P(k)+\Delta T(k)+y(k)*\tau$.

If V(k) is the capacitor voltage at the kth cycle as shown in Fig.2, we could see V(k) signal is generated by V(k-1) and an Ic signal to charge/discharge Cc during up or down signal effective pulse period and an Ib to charge/discharge Cc during kth cycle, i.e., the voltage is determined by three parameters. The change in voltage on Cc for one at kth cycle is :

$\Delta Vf\_a=Ic/Cc*P(k)$.

If the trigger clock is the input modulation signal Ai, then the change in the Cc when charge-discharge is at the kth cycle will be,

$\Delta Vf\_b=y(k)*Ib/Cc*[T(k)+T(k+1)]/2$.

Then,

$\Delta Vf=\Delta Vf\_a+\Delta Vf\_b$,

$V(k+1)=V(k)+\{y(k)*(Ib/Cc)*[T(k)+T(k+1)]/2\}+\{Ic/Cc*P(k)\}$.

Because the maximum frequency shift is much smaller than carrier frequency, the T(k) is approximately equal to carrier cycle Tc and

$V(k+1)=V(k)+Ic/Cc*P(k)+y(k)*(Ib/Cc)*Tc$.

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Assume A=Ic/Cc and B=(Ib/Cc)*Tc. Then,

V(k+1)=V(k)+A*P(k+1)+B*y(k) .

Inserting P(k+1) into the above formula, we get

V(k+1)=V(k)+A*[P(k)+ ΔT(k)+y(k)*τ]+B*y(k)

The quantized output of V(k), y(k) is the total system output.

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Referring to Fig.3, the system structure of digital FM demodulator according to the present invention is shown. This diagram illustrates a two level delta-sigma structure developed from the analysis above. The input is ΔT(k), the signal difference of [illegible] and T(k-1).

In concept, the output signal, y(k), of the present invention is similar to a conventional [illegible]-digital converter output signal. In both systems, the quantized noise signal is [illegible]ed into the high frequency region. However, in conventional systems, the output digital signal y(k) is first accumulated and then filtered from quantized noise by a digital filter to get the modulation signal. This technology is similar to conventional delta-sigma analog-to-digital converters. As shown above, the output digital signal is produced by differentiation of the original modulation signal. In the system of the present invention, the y(k) signal is filtered out of the quantized noise by way of a low-pass digital filter before signal accumulation.

The present invention provides an FM digital demodulator with advantages over conventional technology as follows:

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1. T method and circuit of the present invention is applicable in radio communicati ystems, such as pagers, cellular phones, GPS systems, and DECT systems.

2. T e present invention provides a digital modulation demodulator which adapts I. structure and utilizes the concept of delta-sigma analog-to-digital conve without requiring external components or a high frequency reference cloc as to allow ease of integration.

3. present invention provides a digital modulation demodulator with the functions modulation and analog-to-digital conversion. The input of intermediate- uency signal passes through the inventive demodulator and generates a d l signal including high-frequency quantization noise. Then, by way of an in t low-pass filter, the quantized noise signal is filtered to acquire th seban nal.

Many c es and modifications in the above described embodiment of the invention ca ourse, be carried out without departing from the scope thereof. Accordingly, promote the progress in science and the useful arts, the invention is disclosed s intended to be limited only by the scope of the appended claims.